512 Kbit / 1 Mbit / 2 Mbit Serial Flash
SST45VF512 / SST45VF010 / SST45VF020

Advance Information

FEATURES:

- **Single 2.7-3.6V Read and Write Operations**
- **Serial Interface Architecture**
  - SPI Compatible: Mode 0 and Mode 3
- **Byte Serial Read with Single Command**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 20 mA (typical)
  - Standby Current: 10 µA (typical)
- **Sector or Chip-Erase Capability**
  - Uniform 4 KByte sectors
- **Fast Erase and Byte-Program:**
  - Chip-Erase Time: 70 ms (typical)
  - Sector-Erase Time: 18 ms (typical)
  - Byte-Program Time: 14 µs (typical)
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Software Status
- **10 MHz Max Clock Frequency**
- **Hardware Reset Pin (RESET#)**
  - Resets the device to Standby Mode
- **CMOS I/O Compatibility**
- **Hardware Data Protection**
  - Protects and unprotects the device from Write operation
- **Packages Available**
  - 8-Pin SOIC (4.9mm x 6mm)

PRODUCT DESCRIPTION

The SST45VF512, SST45VF010 and SST45VF020 are manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The Serial Flash is organized as 16 sectors of 4096 Bytes for SST45VF512, 32 sectors of 4096 Bytes for the SST45VF010 and 64 sectors of 4096 Bytes for the SST45VF020. The memory is accessed for Read or Erase/Program by the SPI bus compatible serial protocol. The bus signals are: serial data input (SI), serial data output (SO), serial clock (SCK), write protect (WP#), chip enable (CE#), and hardware reset (RESET#).

The SST45VFxxx devices are offered in 8-pin SOIC package. See Figure 1 for the pinout.

Device Operation

The SST45VFxxx uses bus cycles of 8 bits each for commands, data, and addresses to execute operations. The operation instructions are listed in Table 2.

All instructions are synchronized off a high to low transition of CE#. The first low to high transition on SCK will initiate the instruction sequence. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. Any low to high transition on CE# before the input instruction completes will terminate any instruction in progress and return the device to the standby mode.

Read

The Read operation outputs the data in order from the initial accessed address. While SCK is input, the address will be incremented automatically until end (top) of the address space, then the internal address pointer automatically increments to beginning (bottom) of the address space (00000H), and data out stream will continue. The read data stream is continuous through all addresses until terminated by a low to high transition on CE#.

Sector/Chip-Erase Operation

The Sector-Erase operation clears all bits in the selected sector to "FF". The Chip-Erase instruction clears all bits in the device to "FF".

Byte-Program Operation

The Byte-Program operation programs the bits in the selected byte to the desired data. The selected byte must be in the erased state ("FF") when initiating a Program operation. The data is input from bit 7 to bit 0 in order.

Software Status Operation

The Status operation determines if an Erase or Program operation is in progress. If bit 0 is at a "0" an Erase or Program operation is in progress, the device is busy. If bit 0 is at a "1" the device is ready for any valid operation. The status read is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.

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Reset

Reset will terminate any operation, e.g., Read, Erase and Program, in progress. It is activated by a high to low transition on the RESET# pin. The device will remain in reset condition as long as RESET# is low. Minimum reset time is 10µs. See Figure 14 for reset timing diagram. RESET# is internally pulled-up and could remain unconnected during normal operation. After reset, the device is in standby mode, a high to low transition on CE# is required to start the next operation.

An internal power-on reset circuit protects against accidental data writes. Applying a logic level low to RESET# during the power-on process then changing to a logic level high when V_{DD} has reached the correct voltage level will provide additional protection against accidental writes during power on.

Read SST ID/Read Device ID

The Read SST ID and Read Device ID operations read the JEDEC assigned manufacturer identification and the manufacturer assigned device identification codes. These codes may be used to determine the actual device resident in the system.

TABLE 1: PRODUCT IDENTIFICATION

	Byte	Data
Manufacturer's ID	0000 H	BF H
Device ID		
SST45VF512	0001 H	41 H
SST45VF010	0001 H	45 H
SST45VF020	0001 H	43 H

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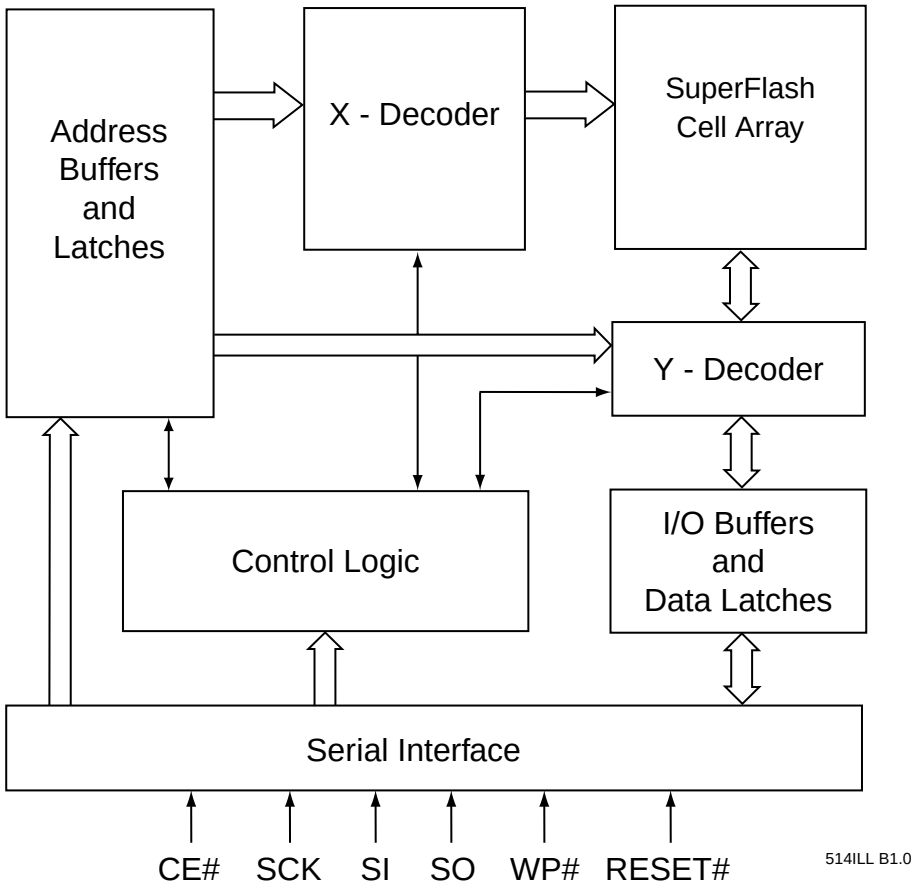
Write Protect

The WP# pin provides inadvertent write protection. The WP# pin must be held high for any Erase or Program operation. The WP# pin is "don't care" for all other operations. In typical use, the WP# pin is connected to V_{SS} with a standard pull-down resistor. WP# is then driven high whenever an Erase or Program operation is required. If the WP# pin is tied to V_{DD} with a pull-up resistor, then all operations may occur and the write protection feature is disabled. The WP# pin has an internal pull-up and could remain unconnected when not used.

FUNCTIONAL BLOCK DIAGRAM



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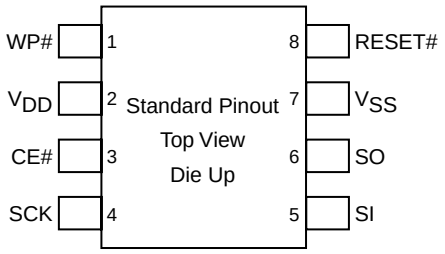

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FIGURE 1: PIN ASSIGNMENTS FOR 8-PIN SOIC

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#.
WP#	Write Protect	To protect the device from unintentional Write (Erase or Program) operations. When WP# is low, all Erase and Program commands are ignored. When WP# is high, the device may be erased or programmed. This pin has an internal pull-up and could remain unconnected when not used.
RESET#	Reset	A high to low transition on RESET# will terminate any operation in progress and reset the internal logic to the standby mode. The device will remain in the reset condition as long as the RESET# is low. Operations may only occur when RESET# is high. This pin has an internal pull-up and could remain unconnected when not used.
V_{DD}	Power Supply	To provide power supply (2.7-3.6V).
V_{SS}	Ground	

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TABLE 3: DEVICE OPERATION INSTRUCTIONS

Bus Cycle	1	2	3	4	5	6	7 and after
Operation/Type	Command	Address[1]	Address	Address	Data	Dummy	Data
Read	FFH	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	X	X	Dout
Sector-Erase[2]	20H	A_{23}-A_{16}	A_{15}-A_8	X	D0H	X	
Chip-Erase	60H	X	X	X	D0H	X	
Byte-Program	10H	A_{23}-A_{16}	A_{15}-A_8	A_7-A_0	Din	X	
Software-Status	9FH	Dout					
Read SST ID	90H	X	X	A_0=0	BFH		
Read Device ID[3]	90H	X	X	A_0=1	Device ID		

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Notes:
1. A_{23}-A_{16} are “Don't Care” for SST45VF512, A_{23}-A_{17} are “Don't Care” for SST45VF010, A_{23}-A_{18} are “Don't Care” for SST45VF020.
2. A_{16}-A_{12} are used to determine sector address, A_{11}-A_8 are don't care.
3. With A_{15}-A_1 = 0, SST45VF512 Device ID = 41H, is read with A_0 = 1.
   With A_{16}-A_1 = 0, SST45VF010 Device ID = 45H, is read with A_0 = 1.
   With A_{17}-A_1 = 0, SST45VF020 Device ID = 43H, is read with A_0 = 1.

TABLE 4: DEVICE OPERATION TABLE

Operation	SI	SO	CE#[1]	WP#	RESET#
Read	X	Dout	Low	X	High
Sector-Erase	X	X	Low	High	High
Chip-Erase	X	X	Low	High	High
Byte-Program	Din	X	Low	High	High
Software-Status	X	Dout	Low	X	High
Reset[2]	X	X	X	X	Low
Read SST ID	X	Dout	Low	X	High
Read Device ID	X	Dout	Low	X	High

Notes:
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1. A high to low transition on CE# will be required to start any device operation except for Reset.
2. The RESET# low will return the device to standby and terminate any Erase or Program operation in progress.

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Advance Information

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{DD} + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{DD} + 1.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 50 mA

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0 °C to +70 °C	2.7-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time ..... 5 ns
Output Load ..... C_L = 30 pF
See Figures 2 and 3

TABLE 5: DC OPERATING CHARACTERISTICS V_{DD} = 2.7-3.6V

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current Read Program and Erase		 20 30	 mA mA	f = 10 MHz CE# = V_{IL}, V_{DD} = V_{DD} Max. CE# = V_{IL}, V_{DD} = V_{DD} Max.
I_{SB}	Standby Current		15	µA	CE# = V_{IHC}, V_{DD} = V_{DD} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{DD}, V_{DD} = V_{DD} Max.
I_{LO}	Output Leakage Current		1	µA	V_{OUT} =GND to V_{DD}, V_{DD} = V_{DD} Max.
I_{IL}	Input Low Current(2)		360	µA	WP#, RESET# = GND
V_{IL}	Input Low Voltage		0.8	V	V_{DD} = V_{DD} Min.
V_{IH}	Input High Voltage	0.7 V_{DD}		V	V_{DD} = V_{DD} Max.
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	V_{DD} = V_{DD} Max.
V_{OL}	Output Low Voltage		0.2	V	I_{OL} = 100 µA, V_{DD} = V_{DD} Min.
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH} = -100 µA, V_{DD} = V_{DD} Min.

Note: 1. Outputs shorted for no more than one second. No more than one output shorted at a time.
2. This parameter only applies to WP# and RESET# pins.

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TABLE 6: CAPACITANCE (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

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TABLE 7: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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Note: 1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: AC OPERATING CHARACTERISTICS VDD = 2.7-3.6V

		Limits		
Symbol	Parameter	Min	Max	Units
F_{CLK}	Serial Clock Frequency		10	MHz
T_{SCKH}	Serial Clock High Time	45		ns
T_{SCKL}	Serial Clock Low Time	45		ns
T_{CES}	CE# Setup Time	250		ns
T_{CEH}	CE# Hold Time	250		ns
T_{CPH}	CE# High Time	250		ns
T_{CHZ}	CE# High to High-Z Output		25	ns
T_{CLZ}	CE# Low to Low-Z Output	0		ns
T_{RLZ}	RESET# Low to High-Z Output		25	ns
T_{DS}	Data In Setup Time	20		ns
T_{DH}	Data In Hold Time	20		ns
T_{OH}	Output Hold from SCK Change	0		ns
T_V	Output Valid from SCK		35	ns
T_{WPS}	Write Protect Setup Time	10		ns
T_{WPH}	Write Protect Hold Time	10		ns
T_{SE}	Sector-Erase		25	ms
T_{SCE}	Chip-Erase		100	ms
T_{BP}	Byte-Program		20	µs
T_{RST}	Reset Pulse Width	10		µs
T_{REC}	Reset Recovery Time		1	µs
T_{PURST}	Reset Time After Power-Up	10		µs

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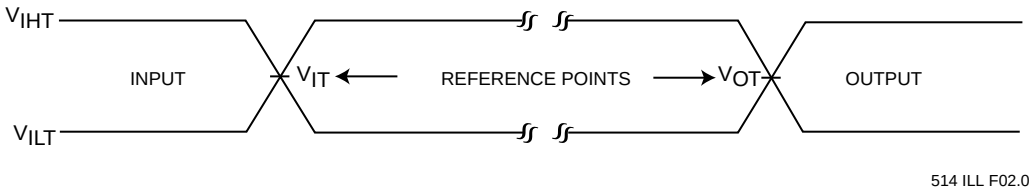


AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0".
Measurement reference points for inputs and outputs are at V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD})
Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT}–V_{INPUT} Test
V_{OT}–V_{OUTPUT} Test
V_{IHT}–V_{INPUT} HIGH Test
V_{ILT}–V_{INPUT} LOW Test

FIGURE 2: AC INPUT/OUTPUT REFERENCE WAVEFORMS

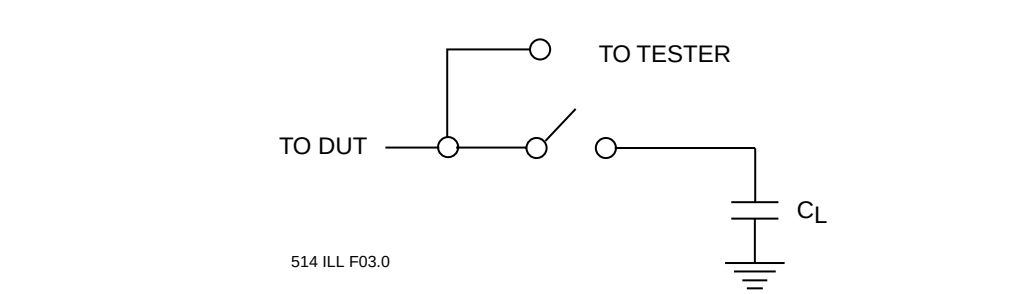


FIGURE 3: A TEST LOAD EXAMPLE

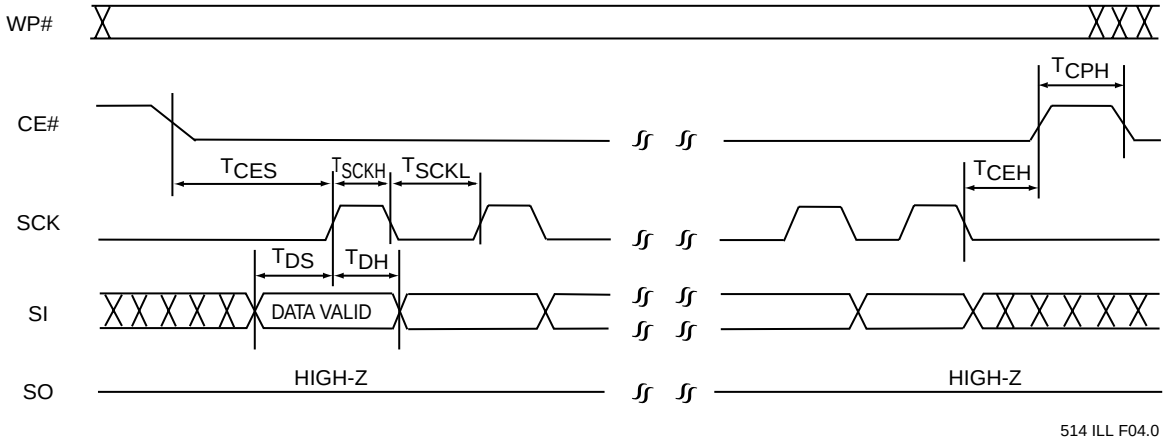


FIGURE 4: SERIAL INPUT TIMING DIAGRAM (INACTIVE SERIAL CLOCK LOW - MODE 0)

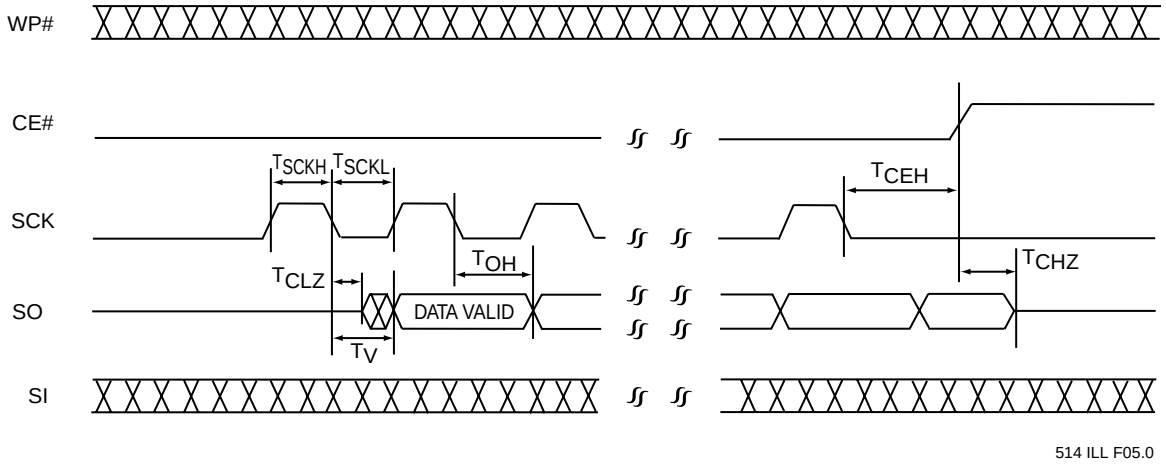


FIGURE 5: SERIAL OUTPUT TIMING DIAGRAM (INACTIVE SERIAL CLOCK LOW - MODE 0)

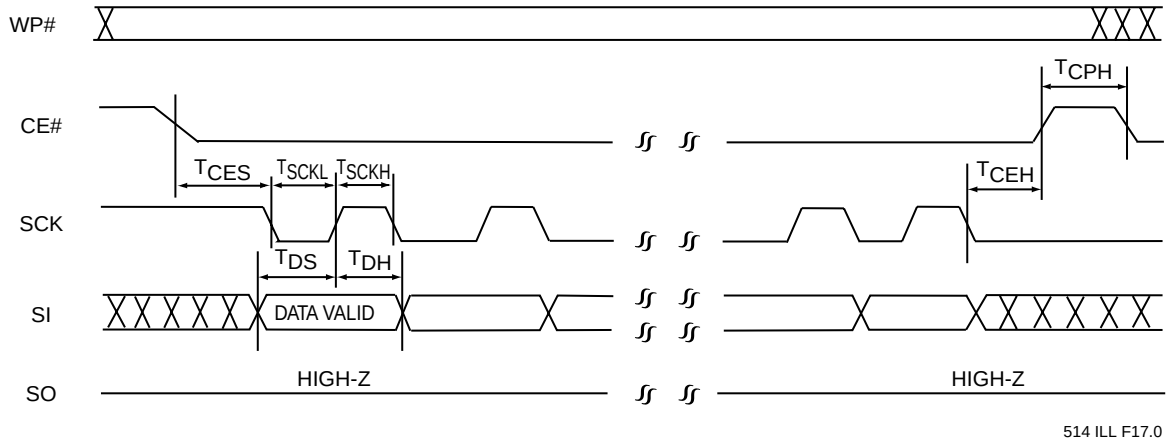


FIGURE 6: SERIAL INPUT TIMING DIAGRAM (INACTIVE SERIAL CLOCK HIGH - MODE 3)

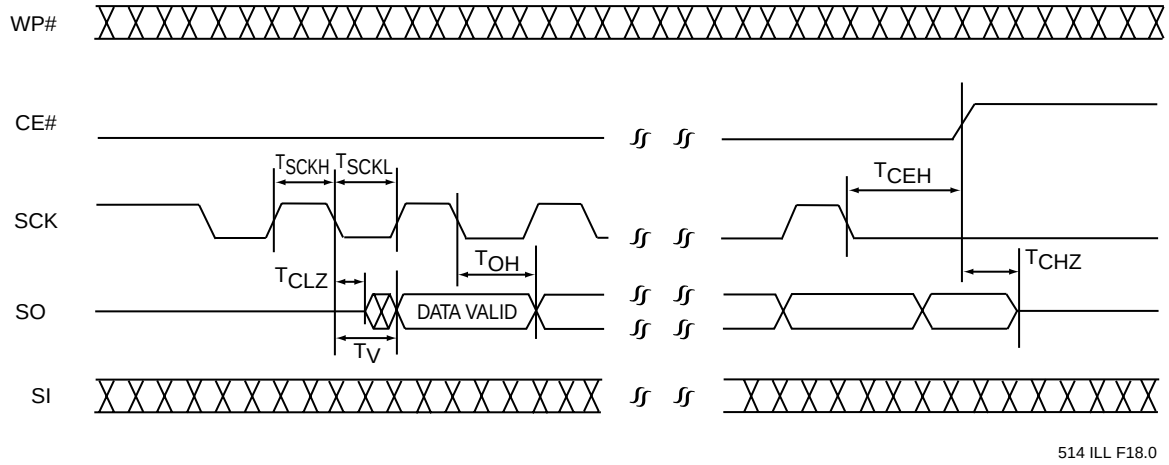


FIGURE 7: SERIAL OUTPUT TIMING DIAGRAM (INACTIVE SERIAL CLOCK HIGH - MODE 3)

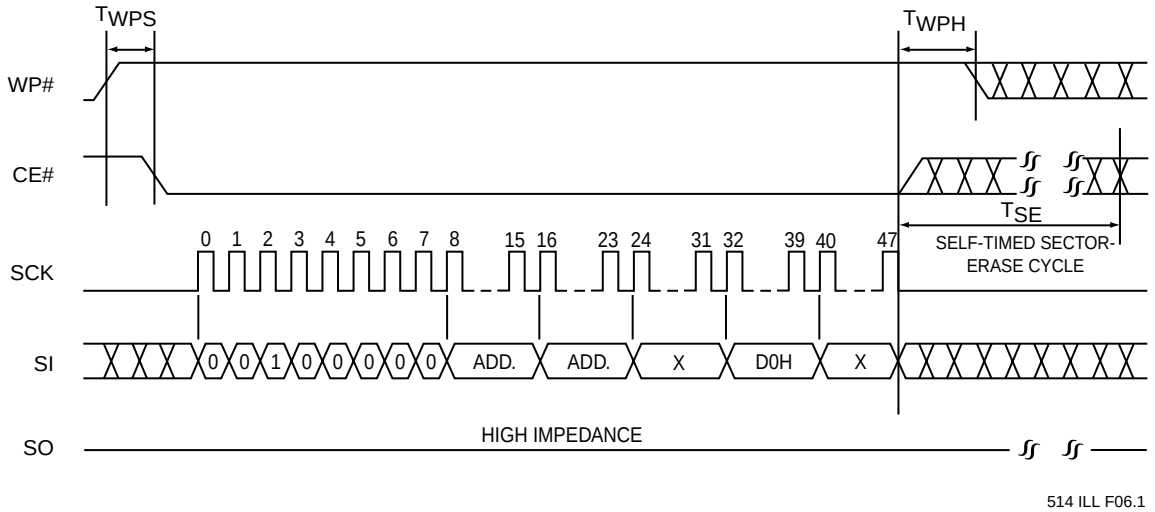


FIGURE 8: SECTOR-ERASE TIMING DIAGRAM

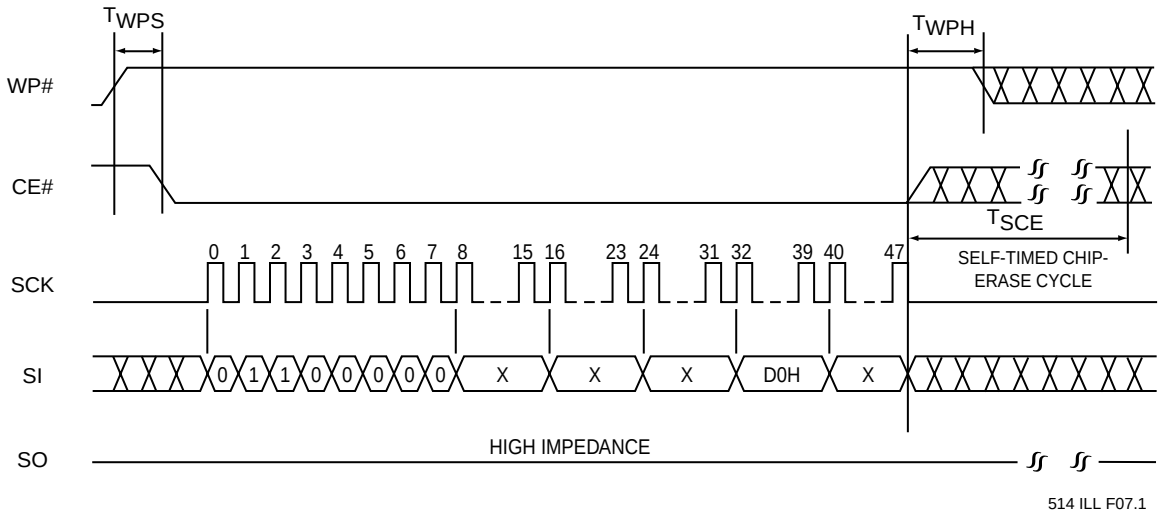


FIGURE 9: CHIP-ERASE TIMING DIAGRAM

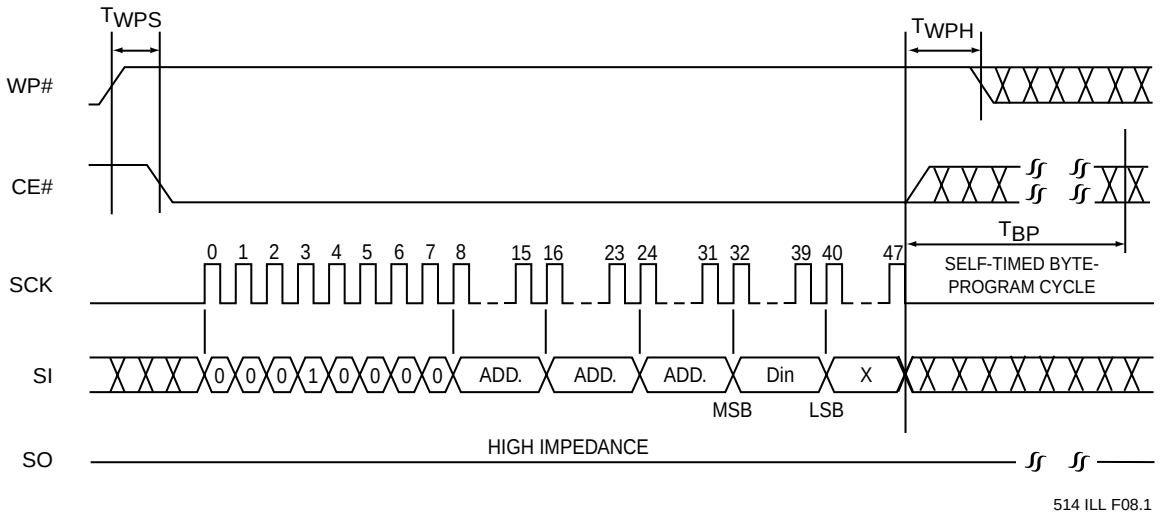


FIGURE 10: BYTE-PROGRAM TIMING DIAGRAM

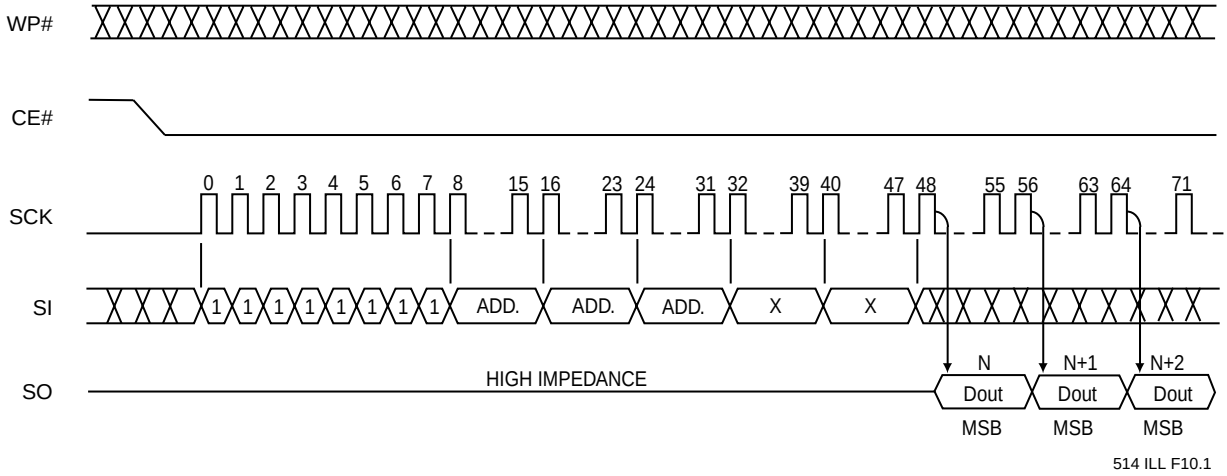
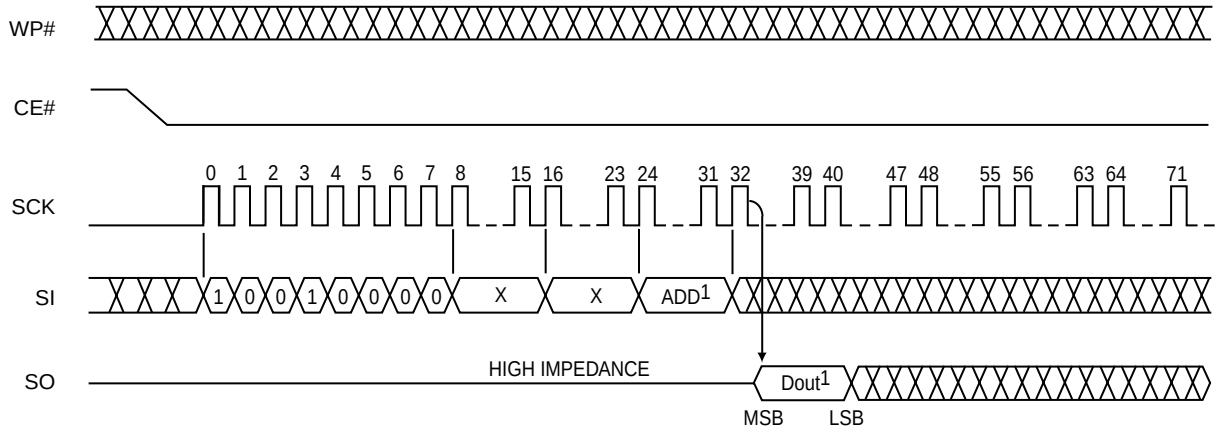


FIGURE 11: READ TIMING DIAGRAM



Note: 1. SST Manufacturer's ID = BFH is read with A_0=0
SST45VF512 Device ID = 41H is read with A_0=1
SST45VF010 Device ID = 45H is read with A_0=1
SST45VF020 Device ID = 43H is read with A_0=1

FIGURE 12: READ-ID TIMING DIAGRAM

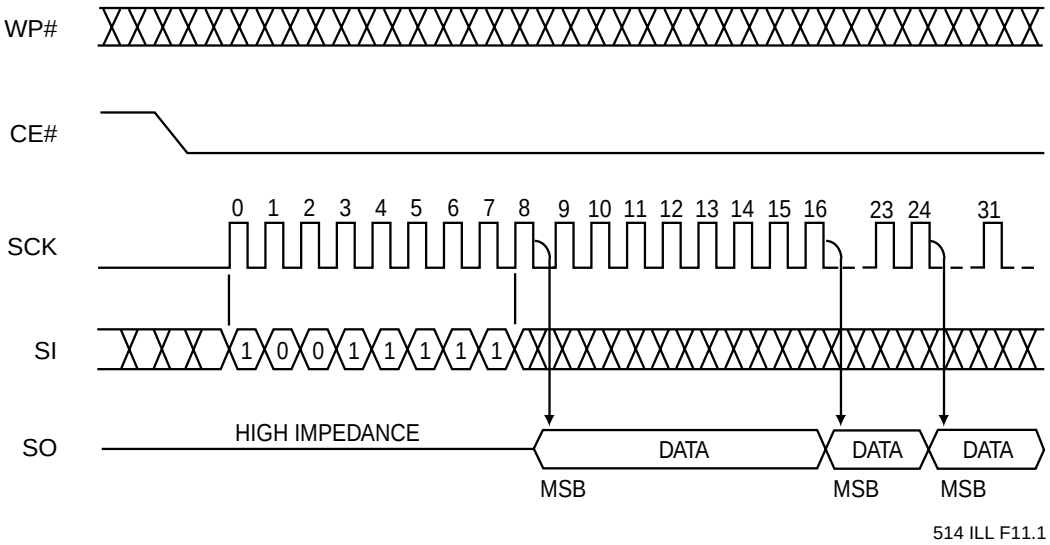


FIGURE 13: SOFTWARE-STATUS TIMING DIAGRAM

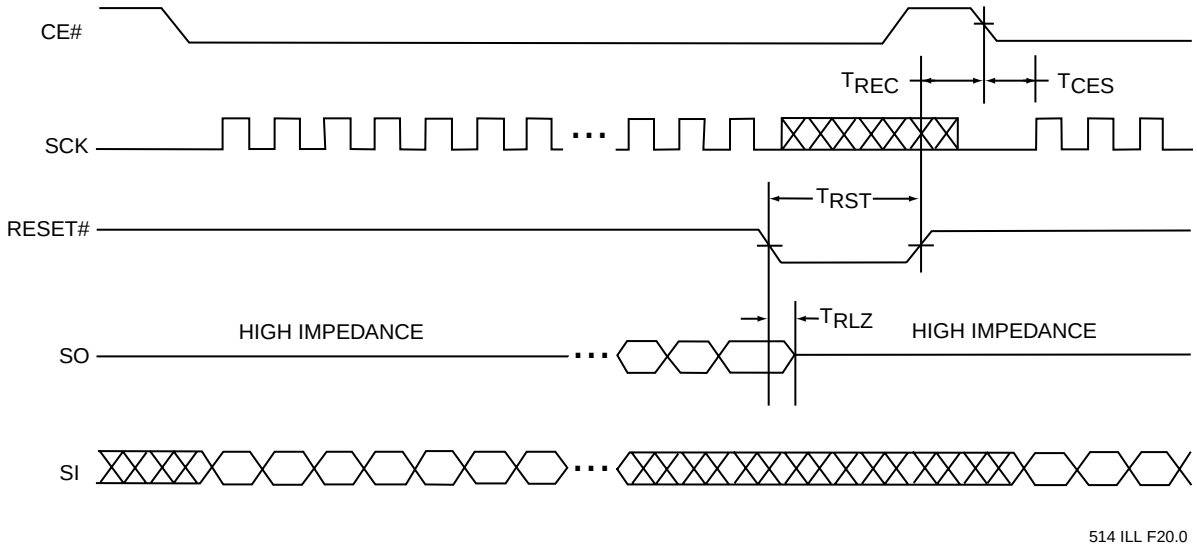


FIGURE 14: RESET TIMING DIAGRAM (INACTIVE CLOCK POLARITY LOW SHOWN)

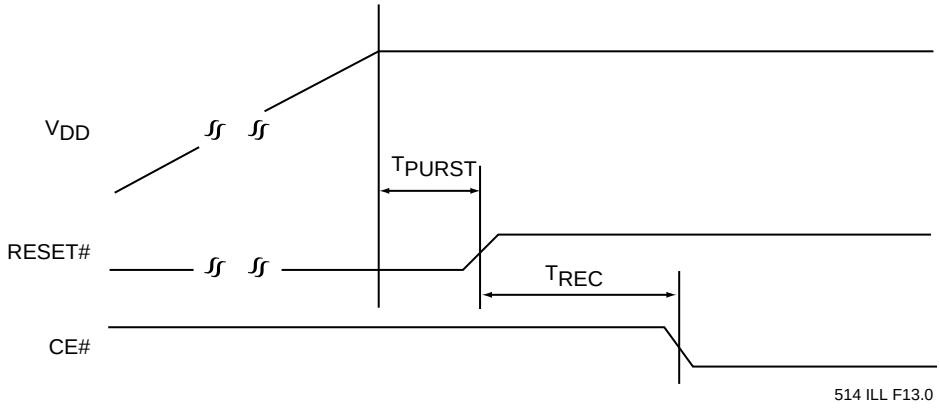


FIGURE 15: POWER-ON RESET TIMING DIAGRAM

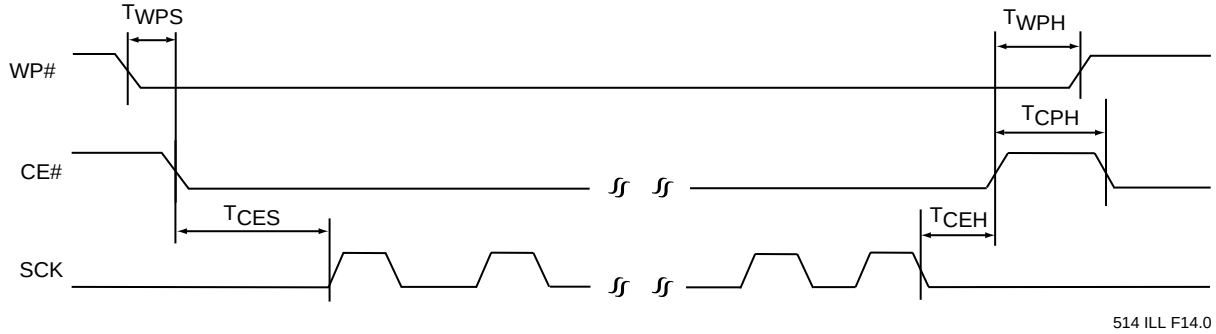


FIGURE 16: WRITE PROTECT TIMING DIAGRAM

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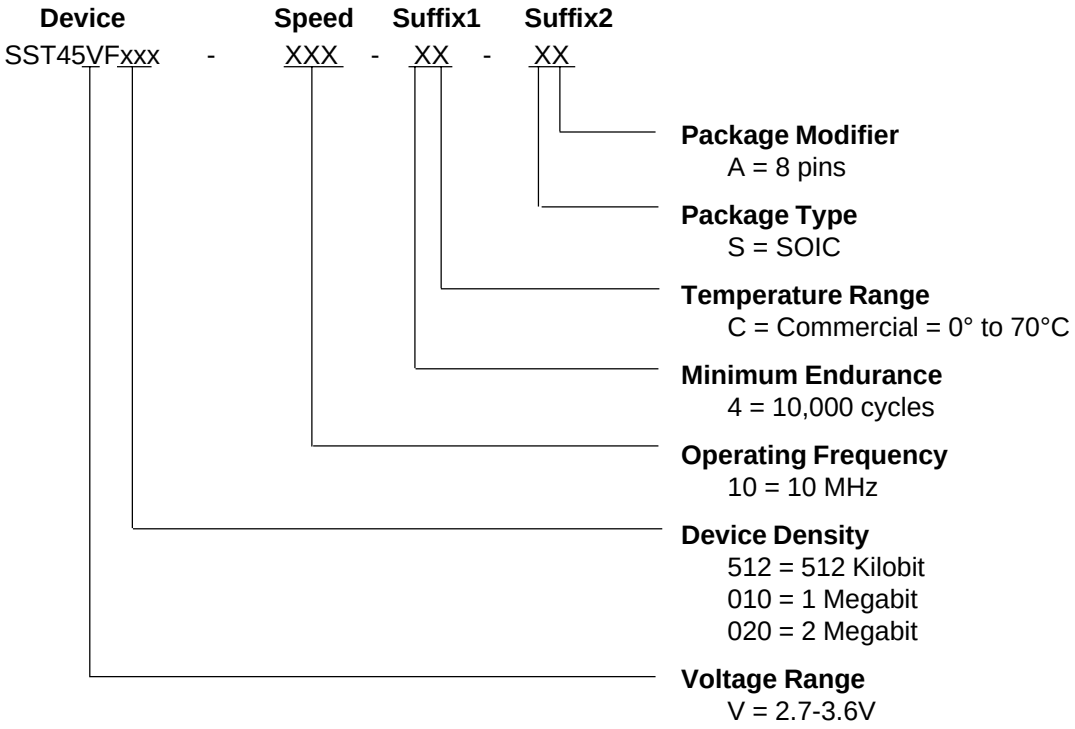

SST45VF512 Valid combinations
SST45VF512-10-4C-SA

SST45VF010 Valid combinations
SST45VF010-10-4C-SA

SST45VF020 Valid combinations
SST45VF020-10-4C-SA

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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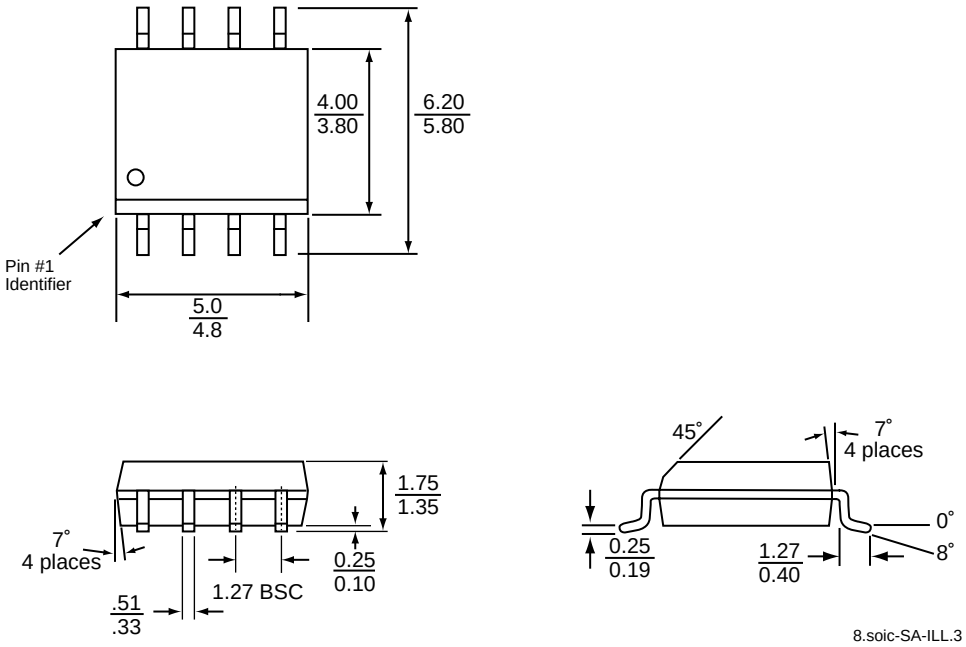
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-012 AA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±.05) mm.

8-PIN SMALL OUTLINE INTEGRATED CIRCUIT PACKAGE (SOIC)
SST PACKAGE CODE: SA

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